P-type InGaAsP Coolers for Integrated Optic Devices

Daryoosh Vashaee[a], Christopher LaBounty[b], Xiaofeng Fanb[b], Gehong Zeng[b], Patrick Abraham[b], John E. Bowers[b], and Ali Shakouri[a]

[a] Jack Baskin School of Engineering,
University of California - Santa Cruz
Santa Cruz, CA 95064-1077, USA

[b] Department of Electrical and Computer Engineering,
University of California - Santa Barbara
Santa Barbara, CA 93106-9560, USA

ABSTRACT

Single stage heterostructure coolers based on thermoelectric and thermionic cooling in p- type InGaAsP superlattice structures have been fabricated and characterized. The effect of ambient temperature and the device size have been studied. Experimental results showed 0.5 degree centigrade cooling below the ambient temperature at 25C. This cooling over 1 mm thick superlattice barrier corresponds to cooling power densities on the order of 200 W/cm^2. The device cools by a factor of two better at higher temperatures (70C). This is due to the reduction of the superlattice thermal conductivity and the broadening of the electronic distribution function at higher temperatures. 150x150 um^2 devices provide largest cooling at room temperature while the optimum device size shrinks as the temperature increases. Simulations results that take into account finite thermal resistance of the InP substrate, the effect of the contact resistance, heat generation in the wire-bonds and metallic pads on top of the device predict accurately the optimum cooling of these micro refrigerators. By eliminating the major parasitic sources of heating (reducing the contact resistance to $5x10^{-7}$ ohm-cm^2, and optimizing the metallic contacts on top of the devices), simulations show that one can achieve up to 15^{o}C cooling (10's of kW/cm^2 cooling power) with single stage p-InGaAsP thin film coolers.

Keywords: Heterostructure cooler, thermionic, thermoelectric, thin film, superlattice, InGaAsP, P-type.

1. INTRODUCTION

Temperature stabilization of optoelectronic components lasers, filters, switches, etc. is of increasing importance in many high-speed and wavelength division multiplexed fiber-optics communication systems. Heat generation and thermal management in very large scale integrated VLSI circuits is becoming one of the barriers to further increase clock speeds and decrease feature sizes. Solid-state coolers integrated with devices is an attractive way to solve some of these problems. This means alternatives to thermoelectric cooling using Bi_2Te_3, the current industry standard, must be found. A solution is to use thermionic emission in heterostructures, a technique that can give significant cooling in conventional materials such as AlGaAs, InGaAsP, or SiGe.[1,2] In this letter, we investigate experimentally and theoretically the thermal behavior of a single stage P-type heterostructure thermionic cooler. The conventional thermoelectric effect is based on bulk properties of materials.[3] When electrons flow from a material in which they have an average transport energy smaller than the Fermi energy to another material in which their average transport energy is higher, they absorb thermal energy from the lattice and this will cool down the junction between two materials. In an alternative method, thermionic emission current in heterostructures can be used to achieve evaporative cooling by selective emission of hot electrons over a barrier layer from cathode to anode.[1,2,4,5] Since the energy distribution of emitted electrons is almost exclusively on one side of the Fermi energy, upon the

Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
2001		**00-00-2001 to 00-00-2001**

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
P-type InGaAsP Coolers for Integrated Optic Devices	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) **Baskin School of Engineering,University of California,Santa Cruz,CA,95064**	8. PERFORMING ORGANIZATION REPORT NUMBER
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited

13. SUPPLEMENTARY NOTES
The original document contains color images.

14. ABSTRACT

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**		**6**	

current flow, strong carrier–carrier and carrier–lattice scatterings tend to restore the quasi-equilibrium Fermi distribution in the cathode by absorbing energy from the lattice, and thus, cooling the emitter junction.

2. EXPERIMENTAL CHARACTERIZATION

In order to investigate experimentally thermoionic emission cooling in heterostructures, a single InGaAsP super lattice barrier surrounded by p^+-InGaAs cathode and anode layers was grown using metal organic chemical vapor deposition (MOCVD). Cathode and anode layer thicknesses were 0.3 and $0.5\,mm$ and and the whole structure was doped to $1x10^{19}$ cm^{-3}. Mesas with an area of 90x180 mm^2 were etched down using dry etching techniques. Ni/AuGe/Ni/Au was used for top and bottom contact metallization. The barrier itself consists of 1 micron thick superlattice (each period is 10nm InGaAs/ 5nm InGaAsP barrier with $l_{gap} = 1.3mm$). In conventional multi-element TE-coolers, cascading of alternate pn-junctions provides the way to send current to an array of coolers electrically in series and thermally in parallel. This way keeps the cooling region far from the joule heating of wire and probes. But in single stage HIT cooler, one has to find a way to send the current to the top of the device. This may be done simply by using a wire bonded to the top contact, but this heats up the device and significantly reduces the cooling power density. An alternate way would be through a side contact with a metal strip connecting the wire bond to the top contact. This keeps the wire bond heat far from the device. This metal strip should be electrically isolated from the bottom of device, so a layer of Silicon-Nitride is deposited underneath. One can see from Fig.1-a that this layer has another benefit which is taking the joule heat of metal down to the substrate as well. It seems this side contact has everything that one may want! Experimental results and data analysis of initial devices showed that this layer bypasses the wire bond heating quite well to the heat-sink, but provides a way to transfer the substrate heat to top contact as well. This will be discussed more in the next section.

Temperature measurements are performed for different size coolers at several stage temperatures. A micro-thermocouple with 25um wire and 50 um tip diameter was used to measure the temperature on top of the device. The device is on a temperature-controlled stage and current is injected through the top contact into the device.

Figure-2 shows the cooling, which is the temperature difference between the top contact and the heat-sink, vs. current. There are various parameters that make the measured data to deviate from ideal behavior. For example the thermocouple on top contact acts as a load connected to the room temperature and makes the cooling results substantially worse for smaller devices. Fig.2-a shows the results at room temperature and Figs. 2-b and 2-c are for the cooling at 50^oC and 70^oC respectively. It turns out that the cooler is working better at higher temperatures, which is quite useful since it makes a negative feedback when used to stabilize the temperature of a load.

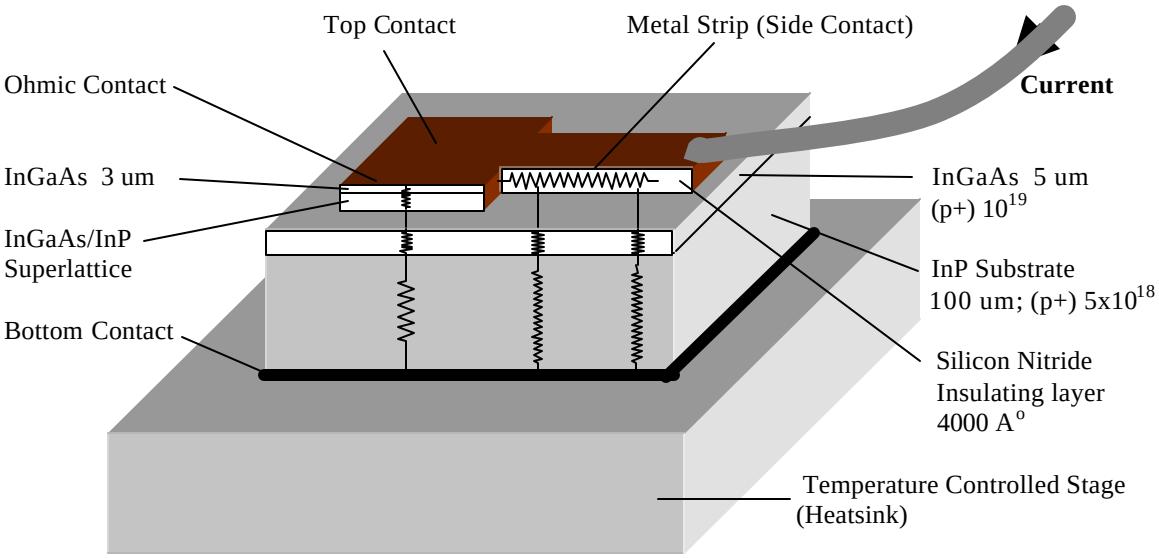
3. THEORETICAL MODELING

In a cooler there are in fact only three sources of cooling against nine sources of heating in the device! Thermoelectric cooling terms are the Seebeck effects in metal-cap layer and in bottom (or buffer) layer-substrate junctions. Thermionic cooling term is at the cap-barrier layer. Assuming small current densities, they are all linearly dependent on current:

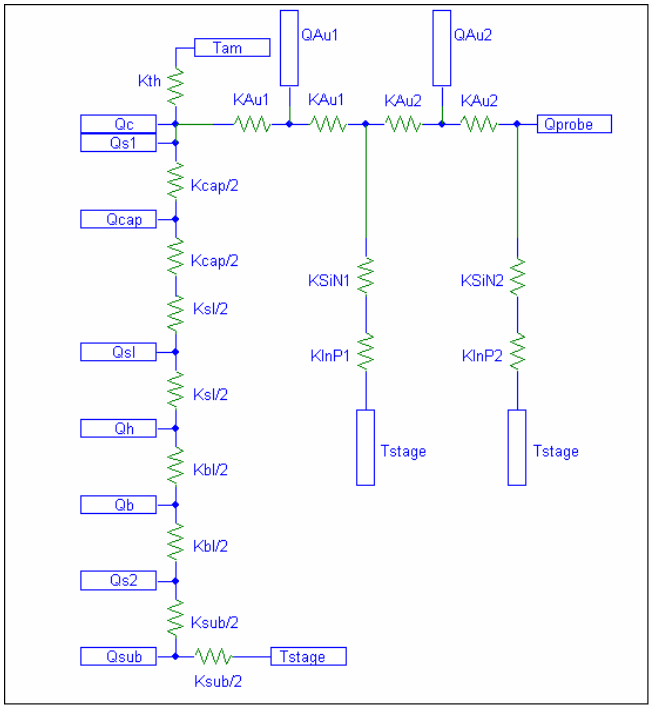
$$\Delta Q = -S_{mc} TI - S_{fs} TI - (f_c + \frac{K_B T}{2q})I$$

where S_{mc} and S_{fs} are the Seebeck coefficients of metal-cap and bottom layer-substrate junctions respectively. Sources of heating are joule heating in the ohmic contact, probe, cap, barrier, bottom layer, and the substrate. The other two "sources of heat" are the ambient heat conduction through the thermocouple contact and the stage heat conduction through the substrate. The last two effects make a zero current temperature difference between the top and bottom contacts, which are not showed in the experimental and simulation curves due to the normalization to zero cooling temperature at zero current. The actual cooling is the temperature difference with respect to that at zero current. The last one is the heat

released in bottom layer by the hot electrons that are coming from the cap layer over the barrier. Thin film cooler works only when its parameters are optimized and outside this range it is nothing but an effectively resistive heater. With optimum current, the cooler is able to provide cooling capacities on the order of couple hundreds W/cm^2.



(a)

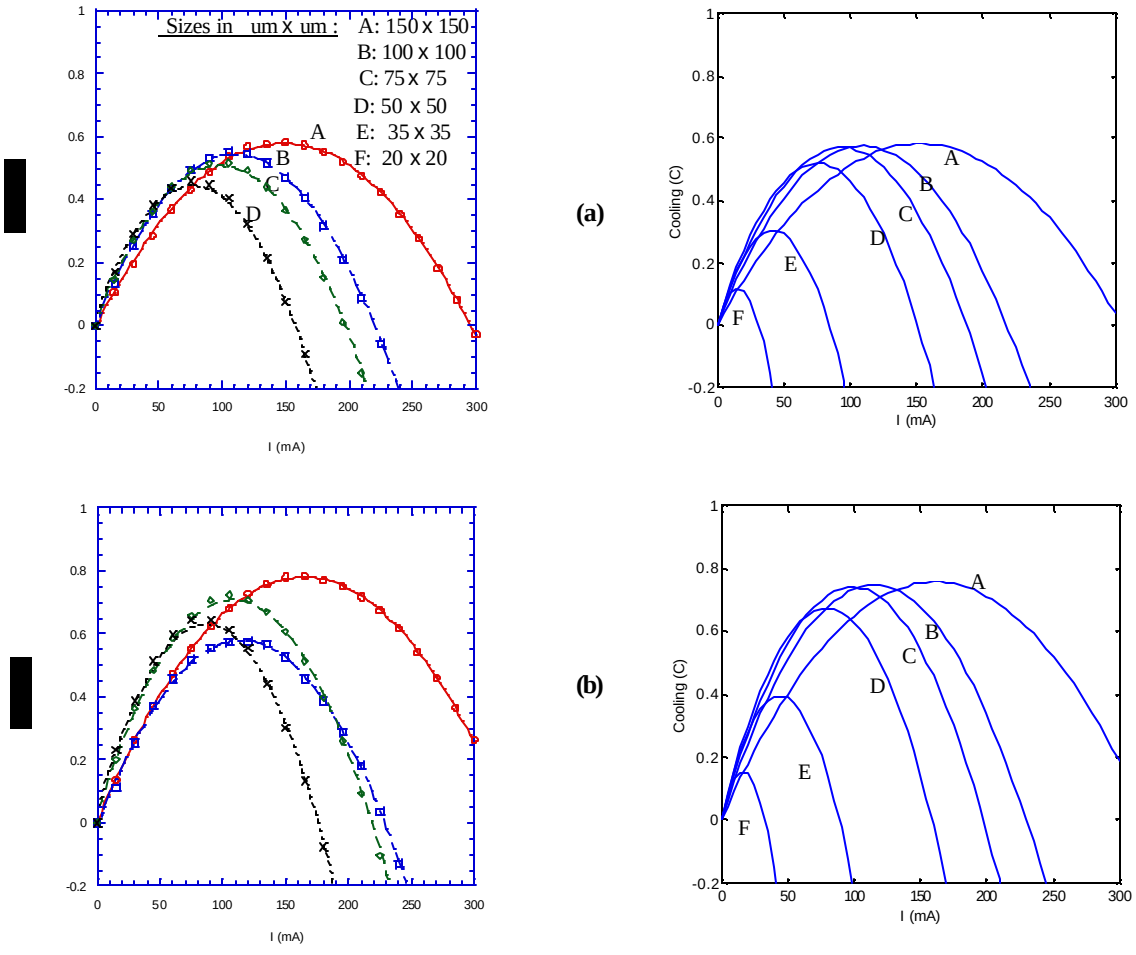


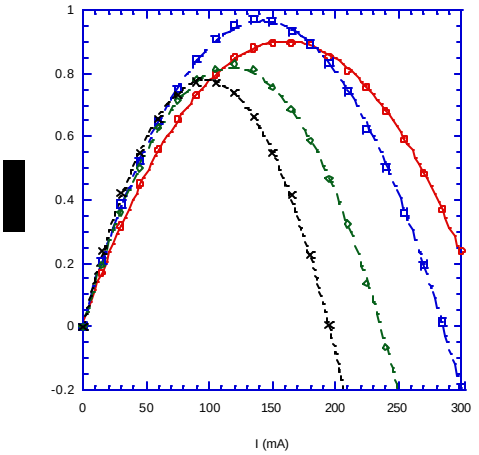
(b)

Figure 1: (a) Device structure showing some important thermal and electrical resistances in the device.
(b) Schematic diagram of the device model.

Fig. 1-b shows the schematic diagram of our model. Resistors represent thermal resistances. *QAu1*, *QAu2*, *Qcap*, *Qsl*, *Qb*, and *Qsub* are different current sources modeling joule-heating terms in the two metal strip sections, cap, superlattice, buffer layer, and substrate respectively. *Qc*, *Qs1*, and *Qs2* are for the different cooling terms of thermionic emission, Seebeck effect at cap-metal junction, and Seebeck effect at bottom (or buffer) layer-substrate junction respectively. *Qh* is the thermionic heating term, and *Tstage* and *Tam* are fixed voltage sources modeling the stage and ambient temperatures. One can show that the joule heating of a resistive media with homogenous heat distribution could be put in the middle of it like an electric current source. Point *C* is on top of the sample where we are interested to know the temperature. Fig.3 shows results for different sizes at different stage temperatures. It turns out that there are three dominant effects heating up the top contact. First one is the ohmic contact resistance of metal-cap interface. The second one is the joule heating inside the substrate, and the third one is the side conduction from the stage through the substrate, silicon-nitride layer and the metal strip of the top contact. We deposit the silicon nitride to make the top metal pad electrically isolated from the bottom, but this layer provides a thermal contact between the top contact and the bottom as well. Side conduction is actually an edge effect that conducts the heat from the buffer layer and substrate to the top or takes the heat from the top metal strip and the top probe to substrate.

Hence, one-dimensional simulation of *SiN* heat conduction effects is not possible, and we utilized an eight-resistor network for a two-dimensional model of the heat flow in this part.





(c)

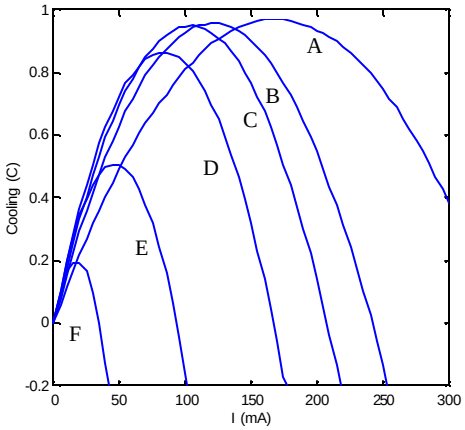
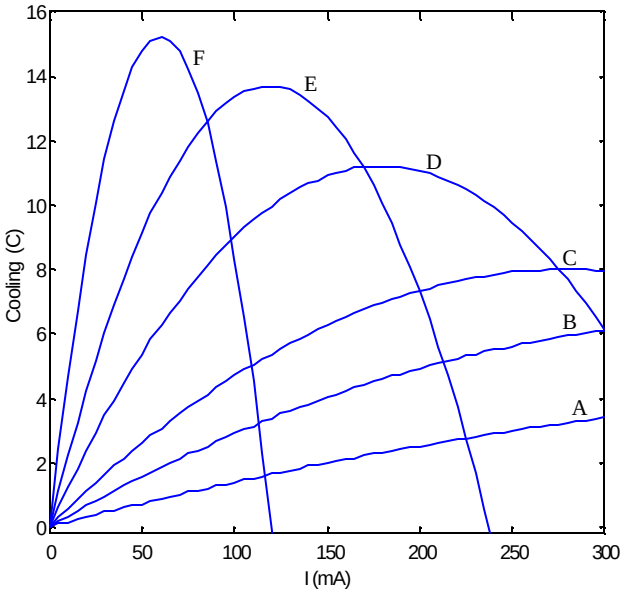


Figure3: Measurements results for cooling of different size devices at (a) room temperature (b) 50C and (c) 70C.

Figure2: Simulation results for cooling of different size devices at (a) room temperature (b) 50C and (c) 70C.

The analysis shows that for small devices, the thermocouple is the dominant limiting factor. It is providing thermal contact through heat conduction to ambient and largely reducing the overall cooling of small devices by reducing the slope of cooling vs. the current. For large devices the optimum cooling occurs at higher currents. Since the heating terms are quadratically dependant on current while cooling terms are linearly dependant, parasitic heating terms (such as contact resistance) reduce the cooling in large devices more than in small devices in which the optimum current is less. As a result, we expect to have a better cooling in small devices, but since the two effects of side conduction and thermocouple heat load are larger for smaller devices and therefore there is an optimum size that turns out here to be around 2500 um^2. This result is valid when the heating of the top contact probe does not affect the device (i.e. probe more than 200-300 um away). Adding this term makes the curves somewhat change depending on the distance of the probe from the top contact. That explains the disordered trends in experimental results compared to the simulation results.

Theoretical modeling of this device predicts that by reducing ohmic contact resistance down to $0.5*10^{-6}$ Ω-cm^2 and by eliminating side-conduction and substrate joule heating, it is able to cool down over 15 degree which corresponds to cooling power densities over 50 kW/Cm^2. Figure 4 shows the predicted curves. Thermocouple effect is excluded in the calculations here.



Sizes in um x um :
A: 150 x 150
B: 100 x 100
C: 75 x 75
D: 50 x 50
E: 35 x 35
F: 20 x 20

Figure 4. Predicted cooling-current curves for different device sizes at room temperature.

4. Conclusion

Heterostructure single-stage coolers based on thermoelectric and thermionic coolings in p-type InGaAsP have been fabricated and characterized. Theoretical simulation that takes into account physical properties of mater, as well as the device geometry and non-ideal effects agree very well with the measured data. Cooling power densities of about 4.5 kW/cm^2 and 2.5 kW/cm^2 have been achieved at room temperature and 70 degree centigrade respectively. Increase of barrier thermal resistance and broadening of electron distribution are the two main reasons for a better cooling at higher temperature. There are nine heating factors limiting the cooling power of the device. Simulation shows the main limiting factors top are metal-InGaAs contact resistance and the side conduction through the insulating silicon nitrade layer. This is the layer isolating the cold side contact from the substrate. Prediction from the simulation shows with the reduction of ohmic contact to 0.5e-6 ohm-cm^2 and with the elimination of side conduction, cooling power densities in the order of 50 kW/Cm^2 can be obtained from P-type InGaAsP coolers.

Acknowledgments

This work was supported by the Office of Naval Research under contract No. 442530-25845, and the Army Research Office through the DARPA/HERETIC program under contract No. 442530-23002.

Refrences:

1. A. Shakouri and J. E. Bowers, "Heterostructure integrated thermionic coolers," Appl. Phys. Lett. **7**1, 1234 (1997).
2. A. Shakouri, E. Y. Lee, D. L. Smith, V. Narayanamurti, and J. E. Bowers, "Thermoelectric effects in submicron heterostructure barriers," Microscale Thermophysical Engineering 2,37 (1998).
3. H. J. Goldsmit, *Electronic Refrigeration* (Pion, London, 1986).
4. G. D. Mahan and L. M. Woods, **"**Multilayer thermionic refrigeration", Phys. Rev. Lett. **8**0, 4016 (1998).
5. G. D. Mahan, J. O. Solo, and M. Bartkowiak, **"**Multilayer thermionic refrigerator and generator", J. Appl. Phys. **8**3, 4683 (1998).